ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes: a device substrate having a semiconductor layer separated by a dielectric layer from a base substrate; a memory cell array having a plurality of memory cells formed and arranged on the semiconductor layer of the device substrate, each the memory cell having a MOS transistor structure with a body in an electrically floating state to store data based on a majority carrier accumulation state of the body; and a sense amplifier circuit configured to perform data read out of the memory cell array, the sense amplifier circuit including a bipolar transistor for performing current amplification of a memory cell selected during data reading.